ABSTRACT OF THE DISCLOSURE

The present invention determines the ESD event by detecting the voltage value of the power source. The numbers N of the diodes 441 have to follow the condition of:

N×VT (0.7) > Vcc (core)

Therefore, the diodes 441 will not influence normal operation outside of ESD events. When an ESD pulse is generated, the PN junction of the PMOS transistor is turned on, so the voltage value of Vcc is raised. At this time, the voltage value of Vcc (core) is "Vcc-0.7-N1×(0.7)", N1 represents the numbers of diodes between Vcc (core) and Vcc, which follows the condition of "N1×(0.7)>Vcc-Vcc (core)" to ensure the diodes remain turned on in normal operation.